The following is a complete listing of all claims in the application, with an indication of the status of each:

Listing of claims:

1. (Currently Amended) A method for evaluating minority carrier transmission in a semiconductor chip design, comprising the steps of:

forming said semiconductor chip design using shapes;

defining an arc between a first point and a second point in said semiconductor chip design, wherein said arc crosses at least one of said shapes;

quantifying absorption, reflection and transmission characteristics of each domain along said arc; ~~and~~

evaluating total minority carrier transmission from said first point to aid second point across said domains using said quantified characteristics [[,]] ; and

determining latchup or noise or defect in said semiconductor chip design based on results of said evaluating step.

2. (Original) The method of claim 1, wherein each of said domains is delimited by two normal planes.

3. (Original) The method of claim 2, wherein each of said two normal planes includes a point co-located on said arc and on a perimeter of a shape.

4. (Original) The method of claim 2, wherein each of said two normal planes includes a bisector of a section of said arc, wherein said section is located between two adjacent points.

5. (Currently amended) The method of claim 1, further comprising ~~the~~ a step of removing shapes that are not in ~~the~~ a substrate prior to said step of defining said arc.

6. (Currently amended) The method of claim 1, further comprising ~~the~~ a step of removing shapes within a well tub of a second doping polarity prior to said step of defining said arc.

7. (Currently amended) The method of claim 1, further comprising ~~the~~ a step of calculating electron current collected at said second point.

8. (Original) The method of claim 1, wherein said first point and said second point lie on a boundary of a circuit.

9. (Currently amended) The method of claim 1, further comprising ~~the~~ a step of relating said arc to a pnpn structure.

10. (Original) The method of claim 1, wherein said step of evaluating is carried out by calculating a transmission matrix for total minority carrier transmission across said domains.

11. (Original) The method of claim 10, wherein said transmission matrix is a higher order matrix.

12. (Currently amended) A method for evaluating minority carrier transmission across an array of unit cells in a semiconductor chip design, comprising the steps of

a) forming said semiconductor chip design using shapes;

b) evaluating, for each of said unit cells, minority carrier transmission across said unit cell by:

defining an arc between a first point and a second point, wherein said first point and said second point are located on a boundary of said unit cell, and wherein said arc crosses at least one of said shapes;

defining one or more domains in relation to points on said arc;

quantifying absorption, reflection and transmission characteristics of each domain along said arc; and

calculating an individual value for minority carrier transmission from said first point to aid second pont across said domains for said unit cell using said quantified characteristics;

c) defining a second arc from a point A to a point B across said array of unit cells; and

d) evaluating total minority carrier transmission along said arc by multiplying together individual values of minority transmission for all unit cells in said array of unit cells along said second arc.

13. (Currently amended) The method of claim ~~10~~ 12, wherein each of said domains is delimited by two normal planes.

14. (Currently amended) The method of claim ~~11~~ 13, wherein each of said two normal planes includes a point co-located on said arc and on a perimeter of a shape.

15. (Currently amended) The method of claim ~~11~~ 13, wherein each of said two normal planes includes a bisector of a section of said arc, wherein said section is located between two adjacent points.

16. (Currently amended) The method of claim ~~10~~ 12, further comprising ~~the~~ a step of removing shapes that are not in ~~the~~ a substrate prior to said step of defining said arc.

17. (Currently amended) The method of claim ~~10~~ 12, further comprising ~~the~~ a step of removing shapes within a well tub of a second doping polarity prior to said step of defining said arc.

18. (Currently amended) The method of claim ~~10~~ 12, wherein said unit cells are parameterized cells.

19. (Currently amended) The method of claim ~~10~~ 12, wherein said array of unit cells is selected from the group consisting of DRAM arrays, SRAM arrays, decoupling capacitors, off-chip driver (OCD) banks, receiver banks, ESD input networks, ESD power clamps, analog circuitry, gate array logic regions, custom logic, voltage islands, wiring bays, fill shapes, p-cell libraries, and periodic circuit functions.

20. (Currently amended) The method of claim ~~10~~ 12, further comprising ~~the~~ a step of relating said arc to a pnpn structure.

21. (Withdrawn) A Computer aided design structure for evaluation of latchup and noise, comprising:

a condition probability generator;

means for relating transmission probability to domains or unit cells, or to domains and unit cells, along an arc; and

Means relating said arc to a pnpn structure.

22. (Withdrawn - Currently Amended) The computer aided design structure of claim ~~10~~ 21, further comprising elements selected from the group consisting of a graphical generator; a technology data file source; a parasitic element identifier; a latchup criteria discriminator[[,]]; a graph theory generator of parasitic pnpn elements; a current generator of secondary currents initiated by elements that undergo latchup; a primary current and secondary currents summing structure; a tree propagation generator; and a latchup propagation evaluator.

23. (Withdrawn) A computer aided design apparatus, comprising:

a graphics generator;

a schematic generator; and

a graphical interface containing a parameterized cell, wherein said parameterized cell is defined by said graphics generator and contains transmission, absorption, and reflection parameters corresponding to said parameterized cell.

24. (New) The method of claim 1, further comprising a step of redesigning said chip to correct latchup or noise or defect determined in said determining step.